

## **TILED MICROELECTROMECHANICAL DEVICE MODULES AND FABRICATION METHODS**

### **Cross-Reference to Related Application**

This application claims the benefit of provisional application Serial No. 60/268,784, filed February 14, 2001, entitled *Tiled Microelectromechanical Mirror Arrays and Fabrication Methods*, the disclosure of which is hereby incorporated 5 herein by reference in its entirety as if set forth fully herein.

### **Field of the Invention**

This invention relates to microelectronic devices and fabrication methods, and more particularly to microelectromechanical devices and fabrication methods.

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### **Background of the Invention**

Microelectromechanical (MEM) devices recently have been developed as alternatives for conventional electromechanical devices, such as relays, actuators, valves and sensors. MEM devices are potentially low-cost devices, due to the use of 15 simplified microelectronic fabrication techniques. New functionality also may be provided because MEM devices can be much smaller than conventional electromechanical devices.

Arrays of MEM devices are widely used for switching, sensing and/or other applications. For example, arrays of microrelays, microsensors, microactuators 20 and/or micromirrors may be used for many applications. More specifically, MEM mirror arrays are widely used, for example, in optical cross-connect (OXC) switches. In a MEM mirror array, an array of moveable mirrors is fabricated in a microelectronic substrate. The mirrors may be moved individually to perform optical switching.

25 Unfortunately, it may be difficult to fabricate large arrays of MEM devices with acceptable manufacturing yields. For example, in a 16 x 16 optical cross-

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connect switch, an array of 256 movable mirrors may be needed. It may be difficult to manufacture such an array with acceptable manufacturing yields.

**Summary of the Invention**

5 Embodiments of the invention can tile multiple MEM device substrates, such as MEM mirror substrates, on a base substrate. Each MEM device substrate can include one or more MEM devices such as mirrors. By including one or a relatively small number of devices on a MEM device substrate, the MEM device substrate can be manufactured with relatively high yield and can be tested prior to tiling onto the  
10 base substrate. The separate MEM device substrates and base substrate can also reduce crosstalk and/or other signal interference which could degrade MEM device operation. Solder bumps and/or other mounting techniques may be used to mount the MEM device substrates onto the base substrate.

15 **Brief Description of the Drawings**

Figure 1 is a cross-sectional view of MEM modules according to some embodiments of the present invention.

Figures 2A-2D are cross-sectional views of MEM modules according to some embodiments of the present invention during intermediate fabrication steps for  
20 forming a deep oxide pad according to some embodiments of the present invention.

Figures 3A-3D are cross-sectional views of MEM modules according to other embodiments of the present invention during intermediate steps of fabricating a mirror according to other embodiments of the present invention.

Figures 4A-4I are cross-sectional views of MEM modules according to yet  
25 other embodiments of the invention during intermediate fabrication steps according to yet other embodiments of the present invention.

**Detailed Description of the Invention**

The present invention now will be described more fully hereinafter with  
30 reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be

5 present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Referring to Figure 1, a plurality of MEM device substrates, such as MEM mirror substrates **120**, are mounted on a base substrate **110**, to form a tiled MEM device module, such as a tiled MEM mirror module **100**. The MEM mirror substrates 10 120 may be mounted on the base substrate **110** using solder bumps **130** and/or other mounting structures. Each MEM mirror substrate **120** can include one or more MEM mirrors, and may be fabricated as will be described below. The base substrate **110** may include mirror electrodes **140** that can be used to control movement of the mirrors in the MEM mirror substrates **120** and can also include driver electronics 15 and/or other microelectronic devices that can be used, for example, in an optical cross-connect switch.

In some embodiments, each MEM mirror substrate **120** can include an array of four mirrors, in two rows and two columns. A 4 x 4 array of MEM mirror substrates **120** may be mounted on a base substrate **110** in four rows and four columns, to 20 provide an array of 256 mirrors for a 16 x 16 optical cross-connect switch. This arrangement can allow higher manufacturing yields than may be obtained with a single array of 256 mirrors in a single MEM mirror substrate. It also will be understood that other numbers of mirrors and MEM mirror substrates may be used. Moreover, a single MEM mirror substrate **120** containing one or more mirrors also 25 may be mounted on a base substrate **110**.

Methods of fabricating tiled MEM mirror modules **100** according to some embodiments of the invention now will be described. In fabricating MEM mirror substrates **120**, a deep oxide pad process may be used. A deep oxide pad process first will be described in connection with Figures 2A-2D. Then, fabrication of a MEM 30 mirror substrate **120** and mounting on a base substrate **110** will be described in connection with Figures 3A-3D and 4A-4I.

Referring now to Figure 2A, a Semiconductor-On-Insulator (SOI) substrate or wafer **200** is provided, that includes a bulk semiconductor region **210**, a thin semiconductor-on-insulator layer **220** and a buried insulator layer **230** therebetween.

Region 210 and layer 220 may comprise monocrystalline silicon, and layer 230 may comprise a buried silicon oxide layer. The design and fabrication of SOI wafers are well known to those having skill in the art and need not be described further herein.

As shown in Figure 2B, a layer of silicon nitride 240 or other masking layer is formed and patterned. As shown in Figure 2C, a Deep Reactive Ion Etch (DRIE) is performed through the exposed SOI layer 220 down to the buried insulator layer 230, to form an array or grating of silicon fingers 250. The array or grating of silicon fingers 250 may be formed, so as to allow thermal oxidation thereof, to form a solid silicon dioxide pad having a relatively large area and a relatively large depth. It will be understood that if silicon fingers 250 are not used, it may be difficult to fully oxidize the large area to the depth of the SOI layer 220, for example to a depth of 20 $\mu$ m. It also may be difficult to form a deep, thick silicon dioxide layer using conventional chemical vapor deposition. In sharp contrast, as shown in Figure 2C, if the silicon fingers 250 are sufficiently narrow, for example 1.8 $\mu$ m wide, and have a sufficiently close pitch, such as a pitch of 3.4 $\mu$ m, the silicon fingers 250 may be fully oxidized and coalesce to form an unbroken outer surface that is coplanar with SOI layer 220.

Referring now to Figure 2D, thermal oxidation is performed to consume the silicon fingers 250 and to produce a pad oxide 260 that can fill the gaps between the fingers 250 due to the increase in volume of silicon dioxide compared to silicon, and that may be planarized to about 2000 $\text{\AA}$ . Stated differently, the dimensions of the silicon fingers 250 of Figure 2C may be selected so as to provide a pad 260 that is fully oxidized and that is of approximately the same thickness (20 $\mu$ m) as the SOI layer 220. It also will be understood that the silicon fingers 250 need not be fully consumed, as long as the pad 260 is sufficiently oxidized to planarize layer 220 and to be released during later processing steps, as will be described below. Finally, a slight rippling of the surface of the oxide pad 260 may be present, as shown in Figure 2D, due to the oxidation of the tips of the fingers 250. This rippling can be reduced, if desired, using conventional planarization techniques.

A deep oxide pad process of Figures 2A-2D may be used to form a MEM mirror substrate 120 using processes illustrated in Figures 3A-3D and 4A-4I. It will be understood that the mirrors that are fabricated in Figures 3A-3D have one degree of freedom (i.e., can be rotated about one axis). However, mirrors with two degrees of freedom also may be fabricated using conventional gimbal structures and used in

embodiments of the invention. The mirror surface may have a thickness of between about 5 $\mu$ m and about 25 $\mu$ m of single crystal silicon, and may be formed in the SOI layer 220, as will be described below. A mirror hinge may be formed of 1.5 $\mu$ m thick polysilicon, which can be deposited to a total thickness variation of 0.05 $\mu$ m as will be

5 described below.

Referring now to Figure 3A, a top view of the SOI layer 220 is shown, in which the nitride mask 240 has been removed, and a pair of deep oxide pads 260 have been fabricated, for example using the fabrication process of Figures 2A-2D. As shown in Figure 3B, anchors 310 and hinges 320 may be formed, for example by 10 depositing, patterning and etching a polysilicon layer. As also shown in Figure 3B, the hinges 320 are formed at least partially on the deep oxide pad 260, so that the deep oxide pad can become the sacrificial release layer for the hinges 320.

Then, as shown in Figure 3C, a silicon trench or moat is etched to define the mirror 330 and a surrounding frame in the SOI layer 220. For example, deep reactive

15 ion etching can be performed that can stop at the buried insulator layer 230, as shown in Figure 3C. Then, as shown in Figure 3D, the buried oxide layer 230 and the oxide pads 260 are etched, to thereby free the hinges 320 and the mirror 330. As will be shown below, the buried oxide layer 230 and deep oxide pads 260 may be etched using a backside etch and/or a frontside etch. Accordingly, a hinged mirror is formed. 20 The thickness of the deep oxide pads 260, which are removed, can allow sufficient space for movement of the hinges 320 during actuation of the mirror 330. For example, a trench of about 20 $\mu$ m in depth may be formed, which may be on the order of ten times thicker than the buried oxide layer 230.

Figures 4A-4I describe additional steps for fabricating MEM mirror substrates 25 120, and for mounting the MEM mirror substrates 120 on a base substrate 110 to form tiled MEM mirror arrays 100 such as those illustrated in Figure 1. As with Figures 3A-3D, a one degree of freedom mirror is shown, but a two degree of freedom mirror can be formed using gimbal structures. Additionally, different thicknesses may be provided for the mirror and the hinge.

30 More particularly, as shown in Figure 4A, an SOI wafer 200 may be provided as was described in connection with Figure 2A. The SOI layer 220 may be between about 5 $\mu$ m and about 25 $\mu$ m thick in some embodiments of the invention. Then, as shown in Figure 4B, the deep oxide pads 260 are formed, for example using a process shown in Figures 2A-2D. Then, in Figure 4C, the polysilicon hinges 320 and anchors

310 may be defined as was described in Figure 3B. The polysilicon hinges 320 and anchors 310 may be of the same thickness or different thicknesses. In some embodiments, a thickness of about 1.5 $\mu$ m may be used.

Then, as shown in Figure 4D, a layer is formed and patterned that can provide

5 an underbump metallurgy (UBM) 410 and a mirror metal 420. As is well known, a UBM may be used as a plating base for plating solder bumps. The mirror metal 420 may provide a reflective surface and/or a stress-relieving surface opposite a second mirror surface (described below). The UBM 410 and mirror metal 420 may be patterned from a single layer, for example comprising gold.

10 Then, referring to Figure 4E, the bulk semiconductor region 210 of the SOI substrate 200 may be etched, for example using deep reactive ion etching (DRIE), to expose the buried oxide layer 230. As shown in Figure 4F, a wet etch and/or other conventional etch may be performed to remove the buried oxide layer 230 and the oxide pads 260. A single etch step also may be used. A second layer of mirror metal

15 430, such as gold, then may be formed on the backside of the mirror 330, as shown in Figure 4G. It will be understood that dual mirror metal layers 420 and 430 may be used to maintain planarization of the mirror by equalizing stress, and/or to provide reflective surfaces on both faces of the mirror. The structure of Figure 4G therefore can provide a complete MEM mirror substrate 120. It will be understood that, as was

20 described above, multiple mirrors may be formed on the MEM mirror substrate 120.

Referring now to Figure 4H, the MEM mirror substrate 120 is mounted onto a base substrate 110, also referred to as an IC/electrode die, for example using solder bumps 130 and/or other conventional techniques. It will be understood that solder bumps may be used, because they can provide a controlled separation between the

25 MEM mirror substrate 120 and the base substrate 110, and also can provide lateral alignment of the MEM mirror substrates 120 relative to the base substrate 110. Electrostatic actuator electrodes 140 and/or other microelectronic devices also may be formed in the base substrate 110. As shown in Figure 4I, adequate space x, such as a 35 $\mu$ m space, may be maintained between the edge of the mirror 430 and the bulk

30 silicon region 210 that remains, so as to prevent the bulk silicon region 210 from shadowing optical reflection from the mirror 330, for a mirror tilt of up to four degrees. For larger tilts, larger gaps may need to be present and/or the bulk silicon layer 210 may be fully or partially removed.

It also will be understood that, although Figures 4H and 4I show only a single MEM mirror substrate **120** flip-chip mounted on a base substrate **110**, multiple MEM mirror substrates **120** may be flip-chip mounted on the base substrate **110**, as was described in Figure 1. Accordingly, MEM mirror substrates may be fabricated with 5 improved yield and then may be packaged to form a larger MEM mirror array that may be used, for example, for optical cross-connect switching.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the 10 scope of the invention being set forth in the following claims.

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